**North SouthUniversity**

Department of Computer Science and Engineering

**Final**,Summer-2017

Course No: **CSE332** Course Title: **Computer Organization and Design**

Time:45 min Full Marks:40

|  |  |  |
| --- | --- | --- |
|  |  |  |
| 1. | Identify the differences between single cycle and multicycle datapath. | 3 |
| 2. | Explain structural hazard with a specific example. | 2 |
| 3. | Consider the following table that provides the time required by each of the 5 stage of two different processor a and b.   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **Processor** | **Instr. Fetch**  (ps) | **Instr. Decode**  (ps) | **EX**  (ps) | **Mem**  (ps) | **Write Back**  (ps) | | **a** | 300 | 400 | 250 | 500 | 100 | | **b** | 220 | 200 | 100 | 150 | 80 |   Answer the following questions…..  **Processor a (single cycle, pipelined)**   * Clock cycle time(Tc) * Time between two consecutive instructions * Assume, there are a set of 10 instructions. Each of them accesses all the stages. Calculate Throughput (Number of instructions per second)   **Processor b (single cycle, pipelined)**   * Clock cycle time(Tc) * Time between two consecutive instructions * Assume, there are a set of 10 instructions. C Each of them accesses all the stages. Calculate Throughput (Number of instructions per second) | 12 |
| 4. | Consider the following MIPS assembly code and assume that we are using pipeline processor. Now answer following questions.  a. Locate the hazards (if any) into the codes. (use circle to locate)  b. How can you solve those?  c. What is the number of clock cycles required to perform the code correctly? Calculate based on your proposed solution in 4b)  d. Is rescheduling possible? if yes, how many clock cycles requiredafter rescheduling  lw$t1, 0($t0)  and $t3, $t1, $t2  sub $t4, $t1, $t3  slt $t0, $t4, $t3 | 10 |
|  |  |  |
| 5. | The instruction formats for a particular 10 bit ISA are provided as below.  **R-type**  *MSB LSB*   |  |  |  |  |  | | --- | --- | --- | --- | --- | | op (2 bit) | rt (2 bit) | rs (2 bit) | rd (2 bit) | sa (2 bit) |   **I-type**   |  |  |  |  | | --- | --- | --- | --- | | op (2 bit) | rt (2 bit) | rs (2 bit) | immediate (4 bit) |   Consider the following set of compiled instructions that will be run into this ISA.  *lw $t1, 0 ($t0) (1)*  *lw $t2, 0($t0) (2)*  *add $t2,$t1,$t2 (3)*  *sw $t2, 0($t0) (4)*  *Now answer the following questions :*  a.Draw a complete single cycle datapath that can perform the above instructions. Show the connectivity, the bus width of the connections (in bits)s.  ***you will be penalized if you draw any unnecessary components or connectivity***  b. The above single cycle datapath has been divided into 4stages for improving the performance through pipelining. This has been done by adding few pipelines registers in between the stages.   1. How many pipelines registers are required? 2. Calculate the width of pipeline registers? 3. Locate the data hazards. 4. Do we need any stalls to run the above code? How many and where? | 13 |
|  |  |  |